# Project Title

<Title>

# Project Members (Max 3 Members)

<List>

# Project Group Name

<Name>

# Project Scope - 19th Nov

<Here define the exact scope of your project. Describe as much as possible. Show functional block diagrams. >

# Micro-Architecture - 6th Dec

<Provide the Block Level Diagram, Detailed RTL level diagram & FSM Details >

# Design Goals & Optimization Strategies - 6th Dec

<Here list your design goals. What are you aiming for : Latency ? Bandwidth ? Timing ? >

<Why are you aiming for your selected particular design goal?>

<What optimization strategies are you planning (as guided by your Design Goals), Compression Trees, Pipelining, ETC >

# Simulation Results - 12th Dec

<Show using plots/other means to show that your design/quantization is indeed providing you with correct/anticipated results>

# Performance Results - 12th Dec

<Report your timing / bandwidth/latency/area> DON’T copy past synthesis report.

<Comment as of you are able to meet your design goals>

# Level of Completeness - Final Submission - TBD (26th Dec)

<Explain as to how much of your planned scope has been completed. What is still left? Is there anything that you are trying to implement but finding it hard to implement ?>

<What is still left>

**CEP (Project Complexity) Attributes - Describe Briefly - Final Submission - TBD (26th Dec)**

| Attribute | Description | Elaborate and justify the level of Attribute achieved in your project. Relate with various portions of the report. |
| --- | --- | --- |
| WP1: Depth of knowledge | The project shall involve in-depth engineering knowledge related to the area of Digital Design.  [WK-4, Engineering Specialization]. | TODO |
| WP2: Range of conflicting requirements | The project has multiple conflicting requirements in terms of optimal usage of resources and performance. | TODO |
| WP5 Extent of applicable codes | The projects expose the students to broadly defined problems which require development of codes that may be partially outside those encompassed by well documented standards. | TODO |
| WP7 Interdependence | The projects shall have multiple components at hardware level and software level for verification and analysis | TODO |

# Annexure-A (Testbench Snapshots)

# Annexure-B (Code)